

METHOD OF MANUFACTURING FLASH EEPROM CELL

Patent number: JP2001217329
Publication date: 2001-08-10
Inventor: RI HIRETSU
Applicant: HYNIX SEMICONDUCTOR INC
Classification:
- international: H01L21/8247; H01L29/788; H01L29/792; H01L27/115
- european:
Application number: JP20000394241 20001226
Priority number(s):

Abstract of JP2001217329

PROBLEM TO BE SOLVED: To provide a manufacturing method of a flash EEPROM cell wherein growth of an oxide film in a dielectric film is restrained, a number of effective channel structure can be increased and reliability of an element can be improved.

SOLUTION: This manufacturing method contains a step for performing a primary heat treatment process after forming a stacked gate structure, wherein a tunnel oxide film 202, a floating gate 203, a dielectric film and a control gate are laminated in a specified region on a semiconductor substrate 201; a step for forming a low concentration source bonding part 210 by implanting low concentration impurity ions in the specified region of the semiconductor substrate 201; a step for performing a secondary heat treatment process after a spacer 211 is formed on a side wall of the stacked gate structure; a step for etching a specified region of the source bonding part 210 in an etching process using a self alignment source etching mask; and a step for performing a tertiary heat treatment process after the source 210 and a drain bonding part 213 are formed by ion-implanting high concentration impurities.

